

M5S Series



H.265/H.264 Encoder SoC with Integrated Fisheye Correction Function

Models		M530S	M550S	M560S
Host Processor		Cortex™ A5 720MHz		Cortex™ A5 900MHz
Video Compression	H.265/HEVC	H.265/HEVC main profile		
		2M@30fps + 1M@30fps	4M@30fps + 1M@30fps	5M@30fps + 1M@30fps
	H.264/AVC	H.264/MPEG-4 AVC (ISO/IEC 14496-10) baseline, main, and high profile		
2M@30fps + 1M@30fps		4M@25fps + 1M@25fps	5M@30fps + 1M@30fps	
	MJPEG	30MPS	60MPS	75MPS
Video Input Interface	Bayer	Up to one 14-bit channel + one 12-bit channel		
	MIPI Rx	Up to one 4-lane channel		
	SubLVDS	Up to one 8-lane channel or two 4-lane channels		
	BT.1120	Up to two channels		
	BT.656	Up to two channels (including one MUX-4 channel)		
	BT.601	Up to two channels		
Max Capture Channel Number		Four channels (up to 1,920 line width for each channel)		
Max Capture Line Width		7,936		
Max Sensor Resolution		7,936x7,936		
Video Output Interface		Support 8-bit BT.656, 16-bit BT.1120, RGB 888, sRGB (i80-50MP), and MIPI Tx up to one 4-lane channel		
Image Signal Processing		Fisheye correction		
		Geometric lens distortion correction		
		Lens shading correction for separated R/G/B component		
		CFA (support Bayer and 2x2 RGB _{I_R} pattern)		
		Multiple shutter frames fusion (up to 120dB)		
		Digital WDR (local tone mapping)		
		Black clamp for separated R/G _R /B/G _B component		
		Fixed pattern noise removal		
		Defect pixel correction		
		Chromatic aberration correction		
		Purple fringe removal		
		Green balance		
		Gamma correction		
		Color correction (2D LUT)		
		Preference color adjustment (3D LUT)		
		Color format conversion		
		Statistic data output for customized 3A process		
		Hue, saturation, and brightness adjustment		
		Contrast enhancement		
		Up to 16x digital gain control for separated R/G _R /B/G _B component		
		Up to 8x white balance gain control for separated R/G _R /B/G _B component		
		2D/3D noise reduction		
		Adaptive weighting edge enhancement		
Motion detection				
De-interlace				
Privacy mask (support arbitrary mask shape)				
Crop, mirror, flip, rotation				
Resize (support arbitrary scaling ratio from 1/4x to 4x, up to four size-down channels simultaneously)				
Video/Audio Analytics		CEVA™ MM3101 128-bit 500MHz DSP		CEVA™ MM3101 128-bit 666MHz DSP
Audio Interface		Built-in audio codec. Full duplex Single-ended stereo line-in/line-out x1, 16/32ohm single-ended stereo headphone-out x1, Mono microphone input x1, Stereo PDM (digital microphone input) I/F x1 I2S I/F x1		
SDRAM I/F		16-bit DDR3/LPDDR2 SDRAM (up to 500MHz/8Gb) x1	32-bit DDR3/LPDDR2 SDRAM (up to 500MHz/16Gb) x1	32-bit DDR3/LPDDR2 SDRAM (up to 666MHz/16Gb) x1
USB		USB 2.0 OTG x1		
Ethernet MAC		10/100/1000M (support MII, RMII, and RGMII; support TCP segmentation offload; support AVB)		
MMC/SD/SDIO		x2 4-bit or x1 8-bit device, support up to UHS-1 SDXC; one for SDIO only (compliant with SD version 3.01, SDIO version 3.0, MMC version 4.41, eMMC version 4.0)		
NAND Flash		x1 (compliant with ONFi version 2.2)		
UART		x5 Tx/Rx, or x1 Tx/Rx + x2 with hardware flow control		
ADC		x5, 12-bit resolution, one for on-die temperature measurement		
I2C		x3		
RTC		x1 (<5uW@3.3V)		
IrDA		x1		
SPI		x4		
GPIO		Up to 96 bits		
PWM		x12		
XTAL		19.2MHz (for system) and 32.768KHz (for RTC)		
Boot Device		SPI-NOR, SPI-NAND, NAND, SD, USB, UART		
Clock Generator		5 configurable clock sources (support spread spectrum modulation)		
Security		Support SSLv3 and TLS 1.2, Support up to 256-bit on-chip security key encryption/decryption Up to 640 bits write-only OTP memory and 64 bits read-write OTP memory to store security keys and private information		
Operating Voltage		Core: 1.0V, I/O: 1.5V (for DDR3) or 1.2/1.8V (for LPDDR2) and 3.3V		
Process		28nm		
Package		TFBGA361. Ball Pitch: 0.65mm, Dimension: 13mm x 13mm		
Power Consumption		~0.5W	~0.9W	~1.2W
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